Son of Motorola (or, the $20 CPU Chip)

Would you believe – another microprocessor? You bet. The calculator firm, MOS Technology of Norristown, Pennsylvania, has just recently announced a new microprocessor which combines plug in compatibility with the Motorola 6800 and a new instruction set to come out with yet another option for microprocessor users – but at a price of $20 in single quantities. Here comes the under $200 processor kit? Not quite yet, but maybe within a year or two. (It's already to the point where the sheet metal and transformer iron of a home computer often cost more than all the silicon products which make it work . . . this new low on CPU prices just compounds the problem.) It may be three to six months before you see one of these new MCS6501 processors designed into a kit, so Dan Fylstra in his article covers quite a few details of the Motorola 6800 by way of comparison with "Son of Motorola."

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We thought that the "age of the affordable computer" had arrived when you could buy a microprocessor chip for $150. But the potent combination of new technology and free enterprise has brought about developments beyond our wildest expectations.

So now you can buy your microprocessor brand new, in single quantities, for $20. The new offering is from MOS Technology, Inc., and is pin-compatible, but software-incompatible with the Motorola 6800 microprocessor. Although it will be a while before the new chip finds its way into ready-to-build kits for the hobbyist (after all, the first Motorola 6800 kits have just been announced), the news should be of interest to nearly every home brew computer experimenter. So here's a comparison of the Motorola 6800 and the MOS Technology 6500 series, based on the information presently available. If you aren't already familiar with the Motorola microprocessor, don't worry – we'll cover its major features in the course of the comparison.

Hardware Comparison

Both the Motorola 6800 and the MOS Technology chip are TTL-compatible devices, operating from a single five volt power supply. Like earlier microcomputers, such as the Intel 8008, 8080 and National PACE, these processors make use of a bidirectional data bus, to which both memory and input/output devices may be connected. However there are no special input/output instructions in the instruction repertoire of either the Motorola or MOS Technology microprocessors. Output of a character, for example, is accomplished by storing a value into a certain memory location, which is in reality a special register inside an external I/O interface chip, connected to the data bus just like any other RAM or ROM chip.

Motorola supplies a Peripheral Interface Adapter (PIA) chip which connects to the data bus for 8-bit parallel I/O, and an Asynchronous Communications Interface Adapter (ACIA) for bit-serial input/output. (The ACIA is simply a type of UART, as discussed in Don Lancaster's September article on serial interfaces. It may be used to connect a teletype or CRT terminal to the microcomputer system.) MOS Technology plans to supply a similar set of chips.

Most of the time, data is being transmitted between the microprocessor and the memory chips over the data bus. But the processor can also disconnect itself from the bus, enabling, for example, a data transfer to take place directly between an I/O device and memory. Both the Motorola 6800 and the MOS Technology chip have three-state buffers for the eight data lines, enabling them to disconnect from the bus in this fashion. But the Motorola also has three-state buffers on its 16 address lines, whereas the MOS Technology chips do not.

This would be used, for example, in a floppy disk controller which is capable of transferring a whole block of many bytes of data in response to a single command from the CPU. The controller would present a series of addresses on the 16 address lines, and data bytes on the data lines, causing the bytes to be stored in a series of locations in some RAM chip on the bus; all this would take place in the intervals when the CPU itself was disconnected from the bus.

As a practical matter, however, small systems do not require this kind of direct memory access (DMA) capability, and larger systems with more devices on the bus will require buffers on the

Ready or not, here I come: 6800 to 6501.

address lines to supply the necessary power — and these buffers may as well have three-state outputs.

The other major hardware difference between the Motorola 6800 and the MOS Technology 6500 series is that the MOS Technology chip has an 8080-style Ready line, whereas the Motorola 6800 does not. The Ready line is used to make the microprocessor wait for a variable length of time before going on with the execution of an instruction. This feature makes it easy to use the less expensive memory chips, especially for Programmable or Erasable Read-Only Memory (PROM or EROM) which are not as fast as the CPU itself. It is possible to use such devices with the Motorola 6800, of course, by stretching out one of the clock phases to as long as five microseconds. But the availability of the Ready line on the MOS Technology chip is certainly a convenience, and allows you to use extremely slow memories if you wish.

The MCS6501, first in the MOS Technology 6500 series, requires the same type of external clock as the Motorola 6800. But for $25 you can have the MCS6502, which includes an on-the-chip clock, driven by an external single phase clock or an RC or crystal time base input. As the manufacturer suggests, it is probably cheaper in an original design to use the MCS6502 than to provide the external logic to generate the two-phase clock.

To sum up, both the Motorola 6800 and the MOS Technology have comparable features with some differences. In terms of hardware differences, the MOS Technology Ready line is probably more valuable than the three-state address line buffers available on the Motorola 6800.

A final hardware advantage possessed by the MOS Technology chip is speed. The Motorola 6800 cycle time is one microsecond (1 MHz clock rate), and a typical instruction takes about three clock cycles. While the cycle time of the MOS Technology chip is nominally the same, the company has hinted broadly that the chip can be run at clock rates of 2 or even 3 MHz. Of course, one would have to use faster and more expensive memory chips to take advantage of this increased speed.

In addition, certain critical instructions take fewer cycles on the MOS Technology chip. An STA (store accumulator) instruction referencing an arbitrary location takes 4 cycles, versus 5 for the Motorola, and a JSR (jump to subroutine) instruction requires 6 cycles, as opposed to 9 on the 6800. Conditional branches take 4 cycles on the Motorola microprocessor, while they take 2 cycles if the condition is false and 3 if it is true on the MOS Technology chip. Because these instructions are so frequently executed in most programs, the 6500 series should enjoy a performance edge over the Motorola 6800 even at the same clock rate.

Table I. Functionally equivalent instructions for both the Motorola 6800 and MOS Technology MCS6501 microprocessors. The mnemonics are Motorola's. Of course, these instructions operate on the A accumulator only in the MCS6501, but can address either accumulator in the Motorola 6800. The BIT instruction (*) has a different effect on the V and N processor flags in the MCS6501.

ADC	DEX
AND	EOR
ASL	INC
ASR	INX
BCC	JMP
BCS	JSR
BEQ	LDA
BIT*	LDX
BMI	LSR
BNE	NOP
BPL	ORA
BVC	PSH
BVS	PUL
CLC	ROL
CLI	RTI
CLV	RTS
CMP	SBC
CPX	SEC
DEC	SEI
	STA
	STX
	TSX
	TXS

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Software Comparison

We can treat the instruction set architecture of the two processors in two stages, first considering the facilities for manipulating *data* and then dealing with the facilities for manipulating *addresses*. Both features are important to the overall effectiveness of the processor design.

Data Manipulation

The instructions for manipulating data are quite similar on the two processors. There are two major differences: First, the Motorola 6800 has two 8-bit accumulators, A and B, while the MOS Technology chip has only one accumulator, A. Second, in addition to conditional branches for unsigned comparisons, the Motorola 6800 has special branch instructions for signed comparisons, but the MOS Technology chip does not. (The signed comparisons treat the two values as positive or negative numbers in two's complement notation, in the range −128 to +127. For example, −1 is represented as 2^8-1 = 11111111. An unsigned comparison would treat this quantity as the largest possible (8-bit) value, whereas a signed comparison would treat it as smaller than, say, zero.)

Table I lists the instructions which are the same for both processors, while Table II lists instructions on the Motorola 6800 which must be replaced by more than one instruction on the 6500 series microprocessors.

Some of the instructions omitted on the MOS Technology chip are merely incidental; others are more serious. The lack of signed comparisons represents a real inconvenience in many applications. The lack of a simple ADD instruction means that an operation such as A = B + C on one-byte operands must be coded with a "Clear Carry" (CLC) as in this example:

```
CLC
LDA  B
ADC  C
STA  A
```

on the MOS Technology chip. On the other hand, a computation such as A = B + C − D could be coded as

```
CLC
LDA  B
ADC  C
SBC  D
STA  A
```

assuming that the inclusion of "carry" in both operations is indeed desired.

Less serious but still irritating are the absence of the ROR (rotate right), NEG (negate) and COM

Table II. Motorola 6800 instructions which have no direct equivalent in the MCS6501. The information in this table is taken from MOS Technology documentation on the 6500 series.

Motorola 6800 Instruction	Equivalent 6500 Series Sequence
ABA	No B accumulator
ADD	CLC, ADC
BGE loc	BMI *+6, BVC loc, BVS *+4, BVS loc
BGT loc	BMI *+6, BVC *+6, BVS *+6, BVC *+4, BNE loc
BHI loc	BCS *+4, BNE loc
BLE loc	BEQ loc, BMI *+6, BVS loc, BVC *+4, BVC loc
BLS loc	BCS loc, BEQ loc
BLT loc	BMI *+6, BVS loc, BVC *+4, BVC loc
BRA	JMP
BSR	JSR
CBA	No B accumulator
CLR [loc]	LDA #0, [STA loc]
COM [loc]	[LDA loc], EOR #$FF, [STA loc]
DAA	Replaced by SED
DES	Use PHA
INS	Use PLA
LDS loc	LDX loc, TXS
NEG [loc]	EOR #$FF, ADC #1 [or LDA #0, SBC loc]
ROR [loc]	[LDA loc], PHP, LSR, PLP, BCC *+4, ORA #$80, [STA loc]
SBA	No B accumulator
SEV	LDA #1, LSR
STS loc	TSX, STX loc
SUB	CLC, SBC
SWI	BRK saves state without transferring control
TAB	No B accumulator
TAP	PHA, PLP
TBA	No B accumulator
TPA	PHP, PLA
TST	BIT #0
WAI	JMP *
op disp, X [indexed addressing mode]	LDY #disp, op @loc, Y [indirect indexed addressing mode]

(complement) instructions, as well as single-byte instructions to increment and decrement the accumulator. Probably the least significant difference is the omission of the B accumulator on the MOS Technology chip. This is more than made up for by the availability of an extra index register (see below).

All in all, the Motorola 6800 comes out ahead when considering facilities for manipulating data, the most important point in its favor being the availability of the signed comparisons. Generally speaking, however, the basic instructions available on the two processors are quite similar.

Address Manipulation

The greatest architectural differences between the two processors lie in their facilities for manipulating addresses, or their "addressing modes" – and here the MOS Technology chip has much more to offer.

The two microprocessors are the same in one respect: both have special "short forms" of most instructions for referencing the first 256 bytes of memory. This is called "direct addressing" on the Motorola 6800, and "zero page addressing" on the MOS Technology chip. As an example, the most general LDA (load accumulator) instruction is three bytes long; the second and third bytes form the effective address (0-65535), which can reference any byte in memory. The short form of the LDA instruction, however, is two bytes long; the second byte forms the effective address (0-255) of a byte in the first "page" of memory. The "short form" instructions generally take one fewer clock cycle to execute, since only two rather than three instruction bytes must be fetched from memory.

The major differences between the two processors lie in the important area of indexed addressing. The Motorola 6800 has a single 16-bit index register, called X. Essentially all instructions have an indexed addressing form, in which a one-byte displacement (0-255) is added to the address in the index register to form the effective address. The MOS Technology chip, on the other hand, has two 8-bit index registers, called X and Y. All of the computational instructions have indexed addressing forms in which either a one- or two-byte base address is added to the contents of either the X or the Y register to form the effective address.

Which approach is the better one? For the purpose of accessing elements of arrays, or tables of many identical elements, the MOS Technology chip comes out way ahead. This is partly due to the lack of certain critical instructions on the Motorola 6800, such as an instruction to add the contents of an accumulator to the index register, or even to transfer the value in the accumulators to the index register.

Suppose that we wish to add the Ith element of an array, S_I, to another variable, T. In general, the array may be located anywhere in memory, and the subscript I may be the result of some calculation done in the accumulators. Letting S denote the address of the zeroth element (the base address) of the array, and assuming that the value of the subscript I is already in the A accumulator, consider the instructions necessary to accomplish this operation on the two processors.

The biggest difference is in the area of addressing modes, an area where the 6500 series devices far outshine the Motorola 6800.