CT-1024 Serial Interface Assembly Instructions

In order for the T.V. Typewriter II to communicate via a three wire system, a phone line or a magnetic tape data storage system, the parallel ASCII data must be broken down into sequential one bit at a time form both when coming out of the keyboard and going into the terminal. The serial interface or UART (Universal Asynchronous Receiver/Transmitter) provides this conversion from the parallel form into a series of properly timed one's and zero's including not only the serial data, but the start, stop and parity bits as well. The reverse is true during the receive mode. The baud rate or speed at which the serial data is transmitted or received, is 110 baud, or if the optional ports are installed, 150, 300, 600 or 1200 baud. There is a provision for "echo" OFF where the data is transmitted to the receiver, but is not put up on the screen until it is transmitted back by the receiver and displayed by the terminal; or "echo" ON where the data is transmitted and simultaneously put up on the screen and is not echoed back by the receiver.

The input/output connections are RS-232 compatible which will attach directly to most couplers and data sets, however, to record on or playback from magnetic tape it will be necessary to build some kind of FSK encoder/decoder system to get the digital data on and off the tape since this is not provided on the interface. The RS-232 pin connections include transmitted data, received data, terminal "ready" and ground. There are no provisions for transmit/receive switching. Data to be transmitted can either be provided by the screen read board or the keyboard. The interface normally monitors the keyboard, however a "ready to send" command from the screen board locks out the keyboard and allows the screen read board to transmit its data.

The entire circuit is built on a 3 3/8" x 9 1/2" circuit board which is plugged onto the main board at connector strips J1 and J2 just behind the cursor and screen read boards. Switch connections to the serial interface board are provided by 12 pin connector JS-1, while the keyboard is plugged onto 12 pin connector JS-2 rather than J9 of the main terminal board as is done if the interface board is not used.

PC Board Assembly

NOTE: Since all of the holes on the PC board have been plated thru, it is only necessary to solder the components from the bottom side of the board. The plating provides the electrical connection from the "BOTTOM" to the "TOP" foil of each hole. It is important that none of the connections be soldered until all of the components of each group have been installed on the board. This makes it much easier to interchange components if a mistake is made during assembly. Be sure to use a low wattage iron (not a gun) with a small tip. Do not use acid core solder or any type of paste flux. We will not guarantee or repair any kit on which either product has been used. Use only the solder supplied with the kit or a 60/40 alloy resin core equivalent. Remember all of the connections are soldered on the bottom side of the board only. The plated-thru holes provide the electrical connection to the top foil.

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( ) Attach all of the resistors to the board. As with all other components unless noted, use the parts list and component layout drawing to locate each part and install from the "TOP" side of the board bending the leads along the "BOTTOM" side of the board and trimming so that 1/16" to 1/8" of wire remains. Solder.

( ) Install all of the capacitors on the board. Be sure to orient the electrolytic capacitors correctly. The polarity is indicated on the component layout drawing. Solder. Be sure one of the two leads of capacitor C12 is inserted in the center pad of the group of seven holes. (TOP side)

( ) Install the transistors and diodes on the board. The diodes must be turned so the banded end corresponds with that shown on the component layout drawing, and the transistors must be turned so its lead configuration matches with that of the board. Solder. Leave about a 1/8" space between Q2 and the circuit board to prevent the transistor's metal case from shorting to the foil of the PC board.

( ) Install all of the integrated circuits on the board being very careful to install each in its correct position. Do not bend the leads on the back side of the board. Doing so makes it very difficult to remove the integrated circuits should replacement ever be necessary. The semicircle notch on the end of the package is used for reference and should match with that shown on the component layout drawing for each of the IC's. Make sure the integrated circuits are down firmly against the board and solder.

( ) Now attach the two fifteen pin female connectors to the board. These must be installed from the "TOP" side of the board and pressed down so the connectors seat firmly against the board. Solder.

( ) Attach the 12 pin connector JS-2 to the circuit board from the "BOTTOM" side making sure to turn it exactly as shown in the component layout drawing. Note that the connector already has the pins installed. Make sure all of the pins are firmly against the nylon support. They can work loose when pressing the connector onto the board. Solder.

( ) The 12 male printed circuit type pins should now be inserted into the blank Molex connector housing that does not have the nylon insulation between the pins. Do not confuse these pins with the crimp type which look very similar. The pins must be inserted from the back side of the connector into the housing until they snap into place. Orient the connector exactly as it is shown on the component layout drawing and install it in the JS-1 position from the "BOTTOM" side of the board.

( ) If you will be using 150, 300, 600 or 1200 baud it will be necessary to install the parts used for the crystal controlled oscillator and its related circuitry. (These are not supplied with the kit.) Also attach a jumper between points A and C on the interface board. If you are not using the optional baud rates and wish to use the standard 110 baud then attach a jumper between points A and B instead of A and C on the interface board.

( ) If you do not have the screen read inserted on the main terminal board it will be necessary to jumper point O to P on the interface board. If you do have the screen read board installed on the main terminal board omit the jumper.

( ) If you want to guarantee that the receiver remains off during a screen read dump, you will probably want to jumper point S to R on the interface board. If high baud rates are used and/or the turn-around time from whatever feeds the terminal is fast you may have to omit this jumper. If so, you must be sure the terminal is not in, the "echo" mode and that whatever feeds the receiver of the terminal doesn't transmit during a screen dump.

( ) It is also necessary to program the interface board for the correct parity and number of bits to be handled. It will be necessary for the user to either know or find out what type of parity and bit number their computer system is using so the correct jumpers may be installed in the interface board. The transmit and receive formats are identical and are programmed with jumpers as follows:

ODD parity	NO bit 8	jumper J to K and jumper I to H and jumper G to F
EVEN parity	NO bit 8	jumper I to H and jumper G to F
NO parity	NO bit 8	jumper I to H
NO parity	bit 8 = l	NO jumpers
NO parity	bit 8 = 0	jumper E to D

( ) The appropriate "keypressed" strobe jumper should be installed. If your keyboard's strobe is negative, solder a jumper wire between pads L and N. Our KBD unit will work in this configuration. Jumpering pad M to N instead is used for positive "keypressed" strobes where the pulse is clean and there is no ringing. The board must not be wired for a negative "keypressed" strobe (L to N) unless the keyboard strobe is truly negative going.

( ) Now that all of the components have been installed on the board, double check to make sure that all have been installed correctly in their proper location.

( ) Now check very carefully to make sure that all components have been soldered. It is very easy to miss some connections when soldering which can really cause some hand to find problems later during the check out phase. Also check for solder "bridges" and "cold" solder joints which are also a common problem.

( ) Looking at the board from the "TOP" side with the connectors at the bottom, press the nylon indexing plug into J2 pin 2.

( ) This completes the circuit board assembly phase of the instructions. This board should not be installed onto the main terminal board until the main board itself is working and has been completely checked out according to the checkout phase of the terminal assembly instructions.

JS-1 Connector Wiring

Connector JS-1 provides several of the control connections to the interface. Using the wiring table below, attach the wires to the female pins of the 12 pin connector supplied with the interface. All of the wires carry low currents and may be #24 gauge or larger. When all of the pins have been attached, insert each into the 12 pin nylon housing from the numbered side making sure you snap each pin into the appropriate hole. Note that the connector block is marked with the assigned pin numbers.

Pin Number	Function
1	Ground bus
2	"Terminal ready" status line – goes high when power is applied to the terminal. You must draw no more than 5 ma. when sensing this line.
3	Ground for 1200 baud
4	Ground for transmitter "OFF"
5	Ground for Receiver "OFF"
6	RS-232 compatible output
7	RS-232 compatible input
8	Ground for Echo "OFF"
9	Ground for 110 baud
10	Ground for 150 baud
11	Ground for 300 baud
12	Ground for 600 baud

Note: If your system requires a "BREAK" key, it can be implemented by connecting +5 volts thru a 100 ohm 1/4 watt resistor to one side of a SPST pushbutton switch. Connect the other side of the switch to the transmit output of the CT-S interface board (JS-1 pin 6).

RS-232 Applications

If you will be using the unit with a standard RS-232 plug, connect the unit as follows:

RS-232		JS-1
Pin 1	ground	Pin 1
Pin 2	transmitted data	Pin 6
Pin 3	received data	Pin 7
Pin 7	ground	Pin 1
Pin 20	"terminal ready"	Pin 2

Checkout and Use

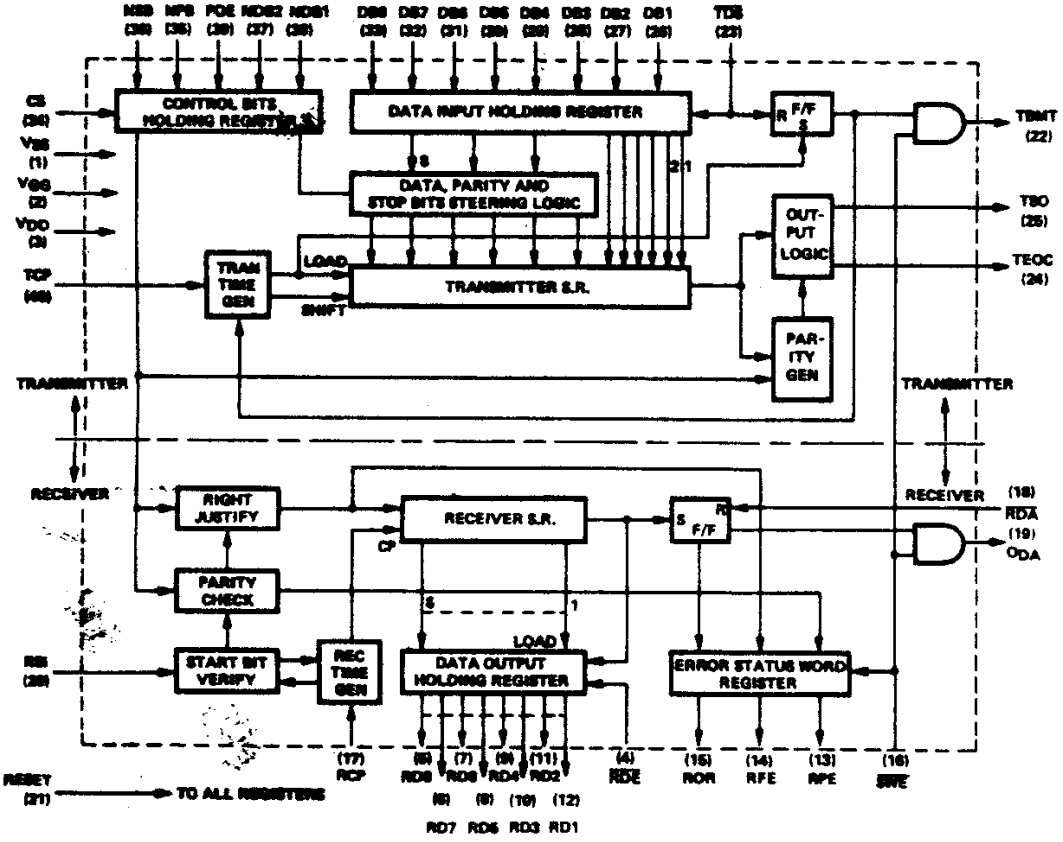
Note that when the interface is used, the keyboard must be plugged into JS-2 on the interface board rather than J9 on the main board. If you will be using the serial interface board along with the screen read board, it will be necessary to attach a jumper from J1 pin 2 to J4 pin 10 of the main CT-1024 board. It is best to use a 3 " piece of #24 wire soldered from the bottom side of the board. This is necessary to make the "START READ" pin functional when the keyboard is plugged into the serial interface board. The easiest way to check the unit out is to operate it with the "echo" ON and the receiver and transmitter switched OFF. This should display everything that is typed on the screen where it can be seen and checked. Since this mode uses both the transmit and receiver circuitry it is a good way to check everything on the interface for proper operation.

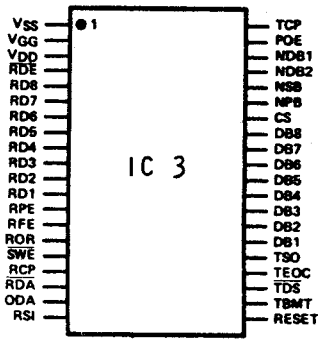
In Case of Problems

If you have problems on some phase of operation of the Serial interface, the best recommendation is to remove power and recheck your assembly over very carefully with the instructions. If you still cannot find the problem and feel secure in your understanding of digital circuits, you can troubleshoot the unit with an oscilloscope. This does, however, require a thorough understanding of how the unit works as is described in the "how it works" section. If you are still not able to locate the problem or prefer not to service the unit yourself, please consult us before sending the unit in for repairs.

Theory of Operation

The serial interface circuit has been designed around a single UART (Universal Asynchronous Receiver/Transmitter) chip which actually does most of the work. The other circuitry on the interface board interfaces the chip itself to the circuitry on the main terminal board. The diagram below shows all of the pin connections to the integrated circuit as well as a block diagram of its internal structure. This is follower by a brief functional description of each of the pins.





PIN DEFINITIONS

Pin	Label	Function
(1)	V_{SS}	+5 Volt ±5%
(2)	V_{GG}	-12 Volt ± 5%
(3)	V_{DD}	Ground
(21)	RESET	A V_{IH} resets all internal registers and counters. The transmitter status outputs TBMT and TEOC are set to V_{OH} indicating the input transmitter buffer register is empty. The TSO output generates V_{OH} or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the V_{OL} state.
(38)	NDBI	Number Data Bits/Character
(37)	NDB2	Number Data Bits/Character
(36)	NSB	Number Stop Bits
		The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs. The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.

NSB	NDB2	NDBI	BITS/CHARACTER	STOP BITS
V_{IL}	V_{IL}	V_{IL}	5	1
V_{IL}	V_{IL}	V_{IH}	6	1
V_{IL}	V_{IH}	V_{IL}	7	1
V_{IL}	V_{IH}	V_{IH}	8	1
V_{IH}	V_{IL}	V_{IL}	5	1.5
V_{IH}	V_{IL}	V_{IH}	6	2
V_{IH}	V_{IH}	V_{IL}	7	2
V_{IH}	V_{IH}	V_{IH}	8	2

(35)	NPB	NO PARITY BIT. A V_{IH} eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a V_{OL} condition.
(39)	POE	PARITY ODD/EVEN. If the NPB input is V_{IL}, the parity mode is ODD if POE is VIL and EVEN if POE is V_{IH}.
		The parity mode is the same for both the transmitter and receiver.
(34)	CS	CONTROL STROBE. A V_{IH} loads POE, NDBI, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER.
		To load the control inputs for static operation CS can be hard-wired to V_{IH}.

(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT
(27)	DB2	HOLDING REGISTER by TDS# Input data must overlap TDS# by 200 nsec.
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit transmitted following the START bit. For data words less than eight bits, the don't care inputs.
(29)	DB4	
(30)	DB5	
(31)	DB6	
(32)	DB7	
(33)	DB8	
(23)	TDS#	TRANSMITTER DATA STROBE. A V_{IL} enters data on the DBI-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V_{OH}, the START bit will be generated on the first negative transition of the input clock TCP following the return of TDS# to a VIH state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V_{OH} (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V_{OH} indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT (S)) is available to load the next character. If a TDS# is not generated within the time allotted, the TSO output will go into an idle state of V_{OH} or a MARK condition. TBMT will remain in the tri state mode unless SWE# is a U_{ZL}.
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V_{OL} to V_{OH} transition indicates the transmission of the character and stop bits have been completed. The V_{OH} is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSL
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V_{IH} to V_{IL} (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.

(12)	RD1	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when RDE# is a V_{IL}. The eight data outputs are in a tri-state mode if RDE is a V_{IH}. Data is presented at the outputs right justified with RDI the least significant bit. For data word lengths less than 8 bits the unused bits will appear as V_{OL}
(11)	RD2	
(10)	RD3	
(9)	RD4	
(8)	RDS	
(7)	RD6	
(6)	RD7	
(5)	RD8	
(4)	RDE#	RECEIVER DATA ENABLE. A V_{IL} enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD 1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V_{OH} indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless SWE# is a V_{IL}. For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.
(18)	RDA#	RESET DATA AVAILABLE. A V_{IL} resets the ODA to a V_{OL}. If ODA is not reset by RDA# the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.
(15)	ROR	RECEIVER OVERRUN. A V_{OH} indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening RDA. If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless SWE# is a V_{IL}.
(14)	RFE	RECEIVER FRAMING ERROR. A V_{OH} indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless SWE is a V_{IL}.
(13)	RPE	RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character does not compare with the parity mode set by POE. RPE will remain in the tri-state mode unless SWE# is a V_{IL}.
(16)	SWE#	STATUS WORD ENABLE. A V_{IL} enables the status outputs ODA, ROR, RFE, RPE and TBMT on the respective output lines. When SWE is V_{IH} all status outputs are in the tri-state mode. For output configurations not requiring a tri-state condition for the status outputs, SWE may be tied directly to ground.

Transmit Mode

Both the outputs from the keyboard and the screen read board are fed into data selectors IC4 and IC10 which select either one of the two sets of inputs with the screen read taking priority. Normally the keyboard is selected as the input, however if the screen read board starts to send data, the incoming normally low to high transition at J2 pin 13 triggers IC7A, a retriggerable 350 ms one shot which selects the screen read inputs and locks out the keyboard, by driving pin 2 of IC4 and IC10 low. It also blocks any data from being received during a screen read if the jumper from S to R is installed, by forcing pin 8 if IC9 A low which gates the "output data available" line into the "reset data available" line of the UART chip. Since the keyboard and receiver are disabled for at least 350 ms after each character dumped during a screen read, there may be problems with a computer sending a return message too soon after the screen read is completed especially when using high baud rates. In these situations, you may not want to lock out the receiver during a screen read transmission and can omit the jumper between points S and R. You must be sure, however, the terminal is not in the "echo" mode and that the computer does not attempt to send data to the terminal until the screen dump has been completed as indicated by an ! transmission if the auto stop function on the screen read board is being used.

Regardless of whether the data to be transmitted comes from the screen read card or the keyboard, it exits from the data selector IC4 pin 12 to IC5 A pin 9 where it is ANDed with the "transmitter buffer empty" output from the UART chip, IC-3, pin 22 where when high, sets the output of the AND gate latch, IC 6 pin 11 high. Each time this IC6 A and B latch is set, it generates a 250 nanosecond pulse thru IC7B providing the "transmitter data strobe" for IC3 pin 23 thus loading the data at the output of the IC4 and IC10 data selectors into the input buffer of the UART chip, IC3. At the fall of the same pulse, a "data accepted" pulse is supplied to the screen read until it resets and forces IC6A pin 9 low which resets the IC6 A and B latch. This reset pulse sent to the screen read board allows it to find and store its next character until the UART transmitter buffer is ready for it. This double buffering enables the transmitter to transmit at up to 1200 baud without gaps or hesitations.

The serial data leaves UART chip, through the "transmitter serial output" IC3 pin 25 where it is ANDed with the transmitter ON/OFF input at IC12C. Transistor Q2 then converts the serial TTL level output to RS-232 formatted data.

Receive Mode

The incoming RS-232 serial data is converted into TTL compatible levels by the Schmitt trigger circuitry IC5 A and its related components, providing approximately 1.5 volts of hysteresis. The output at IC11C pin 8 is then gated with the "receiver ON/ OFF" and ORed with the "echo ON/OFF" and fed onto the UART chip's serial input, IC3 pin 20. When the UART chip sees the stop bits of the character being received, it raises its "output data available" line, IC3 pin 19. If IC9A pin 8 is high, it means the terminal already has a character awaiting loading and is not ready to accept the new character waiting in the "receiver data holding registers". When the character in the terminal's register is finally loaded, the "character accepted" line feeding IC9A pin 11 pulses low toggling IC9A forcing pin 8 low. This allows IC12 to pulse the output of IC5C low clearing the "output data available" line and generating a negative going "keypress strobe" to load the new character into the terminal's data registers. Note that the "keypress strobe" jumper of the main terminal board must be wired for a negative strobe when the serial interface is being used.

If an error is detected by the UART chip, it drives one of three IC3 outputs high. IC3 pin 14 goes high if a stop bit does not follow after the start bit and the correct number of data bits. IC3 pin 13 goes high if there is a parity error received. IC3 pin 15 goes high if there is a condition where the receiver is being sent characters faster than it can accept them. If any one of these three error conditions occurs, transistor Q1 turns on and deselects the receive outputs from IC3 and presents a ? to the terminal as an error indication for the character(s) for which the error was received.

Miscellaneous Circuitry

The standard baud rate for the unit is 110 baud and is derived from the 15840 Hz phase locked oscillator on the main board which is brought in through pin 1 of J1. The 15840 clock frequency is divided by nine by IC2 which gives 1760 Hz required by the UART chip for 110 baud. For higher baud rates a crystal oscillator must be used requiring a 307.200 K Hz crystal as well as ICI and IC8. Inverters IC8 A and B form an oscillator with a frequency of 307.200K Hz which is fed onto flip-flop IC9 B pin 4 where it is divided by two and in turn fed to the programmable divider, IC1 pin 9. By activating the correct select inputs of this integrated circuit, the correct output frequency necessary for each baud rate can be easily set. A five position rotary switch may be attached at jack JS-1 which grounds the selected baud rate line providing easy selection of either 110, 150, 300, 600 or 1200 baud. The 110 baud input inverter also drives the stop bit select line of the UART chip, IC3 pin 36, to select the correct number of stop bits for 110 baud operation.

A "terminal ready" signal is provided at JS-1 pin 2 to tell external devices when the terminal is powered up, however, this output is a sense line only and should not be loaded with anything sourcing or sinking more than 5 Ma.

A power up reset is provided by IC11E to clear out the registers inside of UART chip, IC3, when power is applied to the terminal.

Specifications

Receive Format:	EIA RS-232 and TTL computable with a mark equal to + 1.5 to -25 volts and a space equal to +3 to +25 volts. The range from + 1 .5 to + 3 is the hysteresis region.
Input Impedance:	1.8K ohms
Transmit Format:	EIA RS-232 with a mark equal to -4.7 volts and a space equal to +4.7 volts (2 K ohm load)

Baud Rates -

Standard:	110 baud
Optional:	110, 150, 300, 600, 1200 – selectable

Stop Bits:	Automatic selection of 2 stop bits for 110 baud and 1 for 150, 300, 600 and 1200 baud

Parity -

7 bit	odd, even, none
8 bit	no parity (bit 8 programmable to a 0 or 1)

Parts List - Serial Interface Board (110 baud)

Resistors

R1 – R7, R16, R24	22K ohm 1/4 watt resistor
R8, R15, R17, R20 - R22	
R29, R31, R37, R39, R42	1K ohm 1/4 watt resistor
R9, R27	47K ohm 1/4 watt resistor
R18, R38	12K ohm 1/4 watt resistor
R19	2K ohm 1/4 watt resistor
R23	3.9K ohm 1/4 watt resistor
R25	27 ohm 1/4 watt resistor
R26	2.7K ohm 1/4 watt resistor
R28	5.6K ohm 1/4 watt resistor
R30	330 ohm 1/4 watt resistor

Capacitors

C3	470 pfd capacitor
C4, C6	33 mfd @25 VDC electrolytic capacitor
C5	0.01 mfd capacitor
C7	100 pfd capacitor
C8	0.001 mfd capacitor
C9	330 pfd capacitor
C10 – C13	0.1 mfd capacitor

Transistors and Diodes

D1 – D7	1N4148 silicon diode
Q1	2N5210 silicon transistor
Q2	SS1122 silicon transistor

Integrated Circuits

IC2	7493 4–bit counter
IC3	S1883 UART integrated circuit
IC4, IC10	74157 data selector
IC5	74132 quad schmitt NAND gate
IC6	7400 quad NAND gate
IC7	74123 dual one shot
IC9	7474 dual "D" flip flop
IC11	7404 hex inverter
IC12	7403 quad open collector NAND gate

Note: The S1883 UART chip may be replaced with a Western Digital TR-1602B. The Western Digital TR-1402B and General Instrument AY-5-1013 may also be used. (They produce 2 stop bits at 5 bits / character but this feature is not used in the CT-S)

Parts List – Serial Interface 150, 300, 600, 1200 baud option

Resistors

R10	180 ohm 1/4 watt resistor
R11, R13	1.8K ohm 1/4 watt resistor
R12, R14	470 ohm 1/4 watt resistor
R32 – R36, R40, R41	1K ohm 1/4 watt resistor
R43	2.7K ohm 1/4 watt resistor

Capacitors

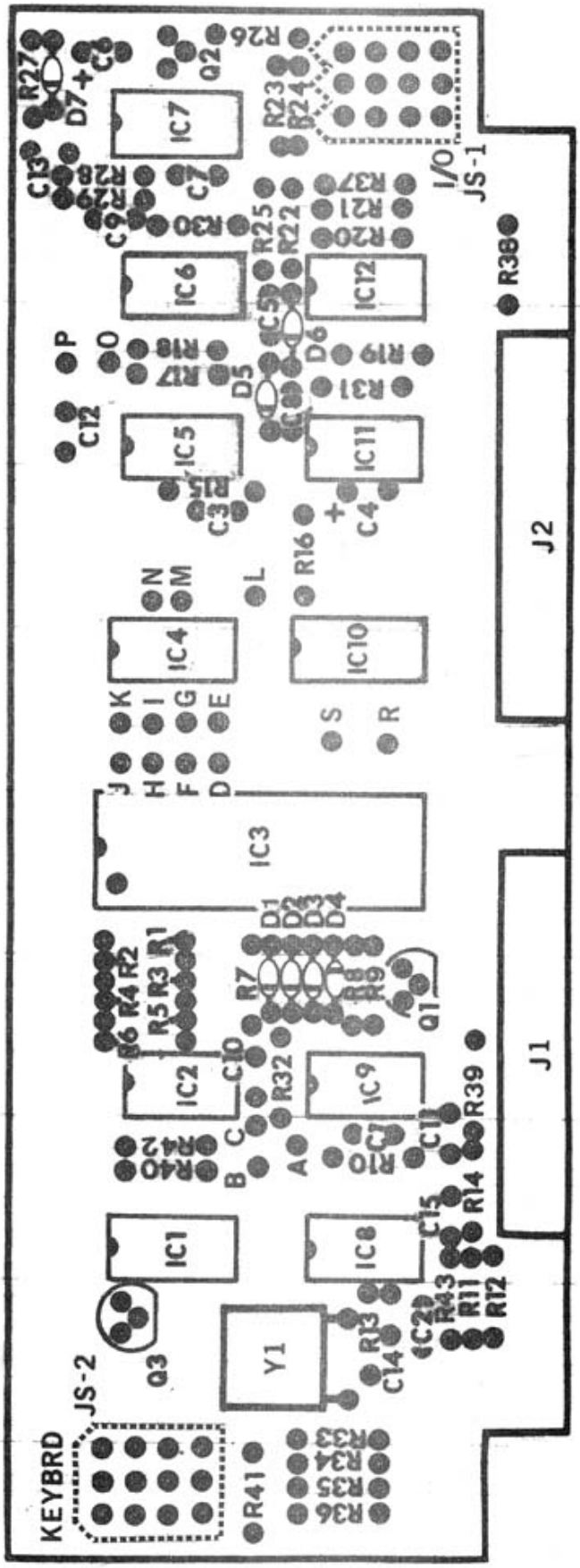
C2	50 pfd capacitor
C1, C14	330 pfd capacitor
C15	0.005 mfd capacitor

Semiconductors

Q3	2N5210 silicon transistor
ICI	7497 6 - bit rate multiplier
IC8	7404 hex inverter

Misc.

Y1	307.200 KHz series resonant crystal



PC Top Layout - Serial Interface Board