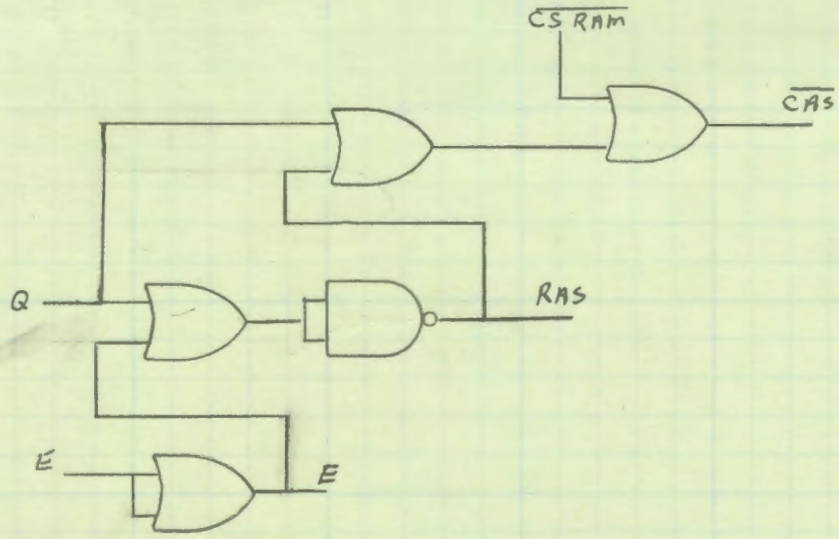
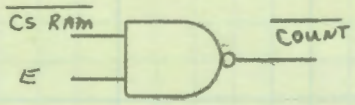
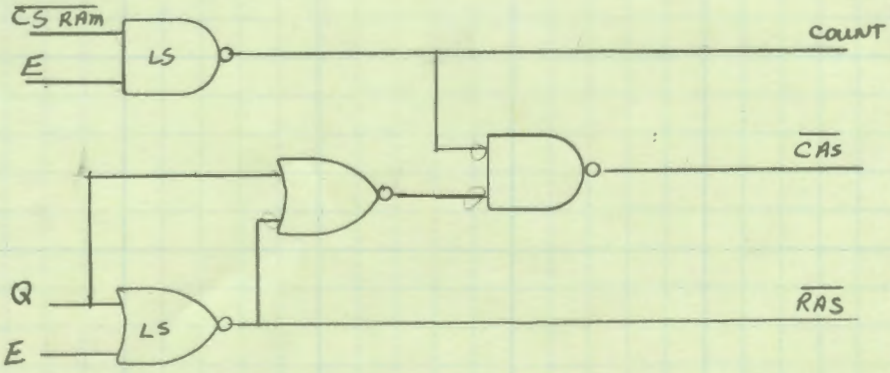
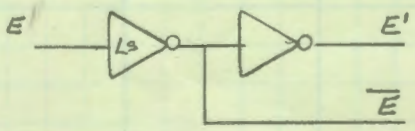
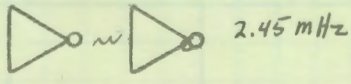




$\overline{\overline{CS\ RAM} \cdot \overline{E}} = CS\ RAM + \overline{E}$







OSC

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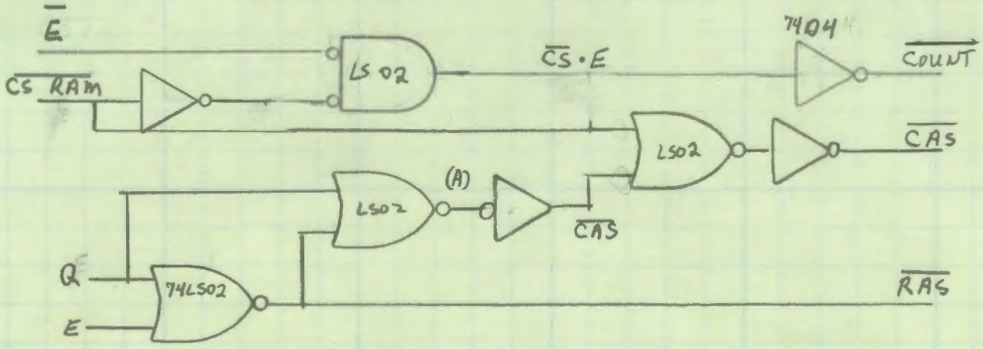
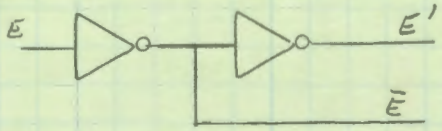
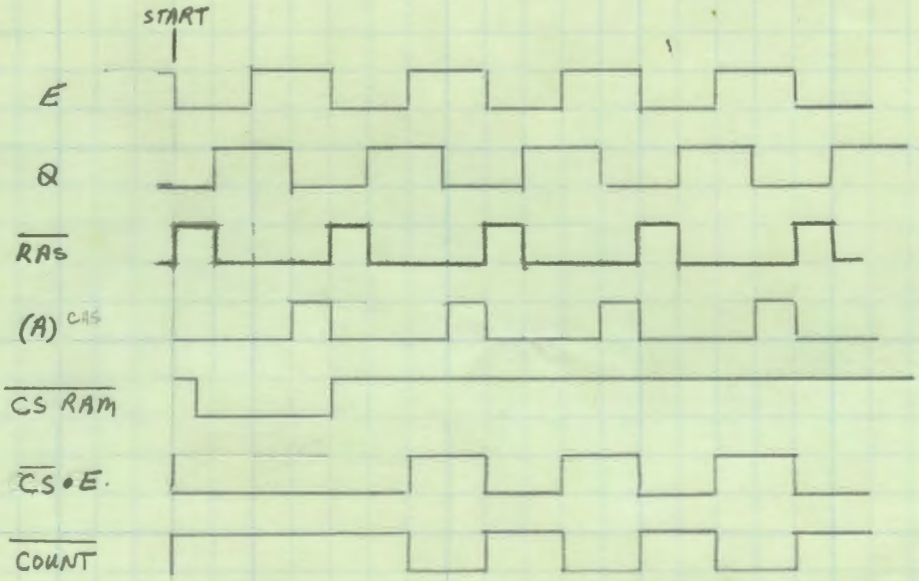
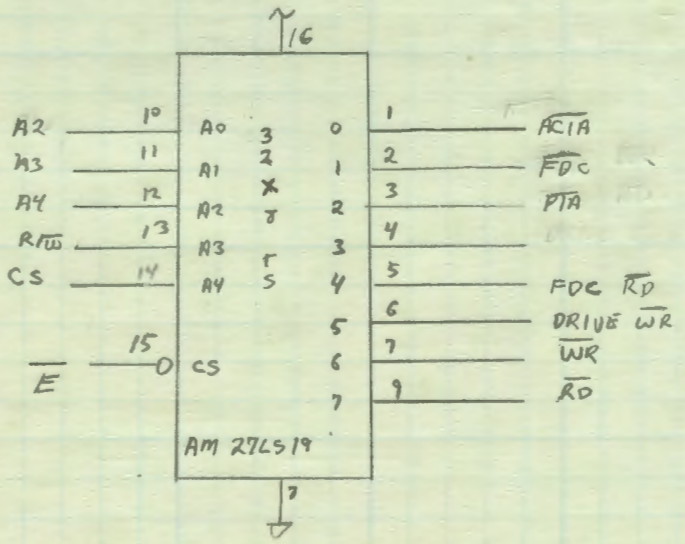

$\overline{E}$
$\overline{CS\ RAM}$
LS 02
$\overline{CS} \cdot E$
7404
$\overline{COUNT}$
LS02
$\overline{CAS}$
LS02
(A)
$\overline{CAS}$
Q
E
74LS02
$\overline{RAS}$


E
E'
$\overline{E}$


START
E
Q
$\overline{RAS}$
(A) CAS
$\overline{CS\ RAM}$
$\overline{CS} \cdot E$
$\overline{COUNT}$


16
A2
10
A3
11
A4
12
R/W
13
CS
14
15
E
A0
A1
A2
A3
A4
CS
3
2
X
T
T
S
0
1
2
3
4
5
6
7
1
2
3
4
5
6
7
9
ACIA
FDC
PIA
FDC RD
DRIVE WR
WR
RD
AM 27LS19
7

1771 CS E018 - E01B

Motor Time Out $\overline{CS}$ 1771 • $\overline{E}$

Motor Reg $\overline{CS}$ E014 • $\overline{WR}$

$\overline{WR}$ $\overline{E \cdot R/\overline{W}}$

$\overline{RD}$ $\overline{E \cdot R/\overline{W}}$

2716 CS FXXX

2K RAM CS E800 EFFF

$\overline{RAS}$ RAS $\overline{E+Q}$

$\overline{CAS}$ RAM • $\overline{Q + \overline{RAS}}$

COUNTER CLK $\overline{E \cdot \overline{CS\,RAM}}$

$\overline{E}$ + CSRAM

$\overline{E} = \overline{Q+E} + \overline{Q}$

$\overline{E} = Q+E \cdot \overline{Q}$

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6809 DECODE PROM

LOC	D3 (I/O)	D2 (RAM2)	D1 (ROM)	D0 (RAM1)	DATA
00 ↕ DF	1	0	1	1	B
E0	0	1	1	1	7
E1 ↕ EF	1	0	1	1	B
F0 ↕ F7	1	1	1	0	E
F8 ↕ FF	1	1	0	1	D